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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/829,479 | 04/22/2004 | Motoo Asai | 251496US90RE | 5882 |

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| EXAMINER | |
|---|---|
| LAM, CATHY FONG FONG | |
| **ART UNIT** | **PAPER NUMBER** |
| 1775 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 01/24/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/829,479 | ASAI ET AL. | |
| | Examiner | Art Unit | |
| | Cathy Lam | 1775 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-92* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-92* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/341,689.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-22-04, 3-31-06*, 9-27-06, 11-24-06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## *Detailed Action*

1. This application is objected to under 37 CFR 1.172(a) as lacking the written consent of all assignees owning an undivided interest in the patent. The consent of the assignee must be in compliance with 37 CFR 1.172. See MPEP § 1410.01.

A proper assent of the assignee in compliance with 37 CFR 1.172 and 3.73 is required in reply to this Office action.

2. The applicant should include any changes, additions, or deletions that were made by a Certificate of Correction to the original patent grant in the reissue application without underlining or bracketing. Certificate of Correction changes and disclaimer of claim(s) under 37 CFR 1.321(a) should be made without using underling or brackets. Since there are part of the original patent and were made before the reissue was filed, they should show up in the printed reissue patent document as part of the original patent.

## *Claim Rejections - 35 USC § 112*

3. Claims 77 and 78 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 77 & 78, in line 3 the phrase "the interposition" lacks antecedent basis.

## *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-20, 23-26, 28-33, 36-42, 48, 52-55, 58, 66, 68, 87-88 and 92 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Nakatani et al (US 5484647).

The present invention regards to a multilayer printed wiring board having a (multilayer) substrate with through hole(s) and an interlaminer insulating layer having conductor circuit formed on the surfaces of the interlaminer insulating layer, is formed both surfaces of the substrate. Via holes are formed in the interlaminer insulating layer. The surfaces of the conductor circuit and the through hole are roughened. A conductive filler is used to fill in the roughened through hole(s). Additional interlaminer insulating layers and conductor circuits are alternately stacked onto both surfaces of the existing interlaminer insulating layers to achieve a multilayer printed wiring board.

Nakatani discloses a circuit substrate comprised of a connecting member (309) and a plurality (or two) printed wiring boards (305) (Fig. 3). The examiner is taking the position that the connecting member (309) is analogous to the presently claimed substrate and the two printed wiring boards are analogous to the claimed interlaminer resin insulating layer.

The connecting member (309) has through holes formed in the thickness direction. A conductive substance is filled into the through holes. The conductive substance is comprised of metallic powder and an epoxy resin (col 5 L 5-12). The connecting member (309) is made from a porous based material, such that surface of the through holes include voids. The examiner is taking the position that the voids

causes the surface to have roughened surface. When the conductive substance (or paste) fills into the through holes, it penetrates to the porous base material side (col 6 L 34-37).

The conductive paste is comprised of metallic powder having an average diameter of from 0.2 to 20 μm (or 200nm-20000nm) and an epoxy resin that can be a bisphenol A epoxy resin (col 9 L 37-38, L 63- col 10 L 19). The examiner is taking the position that the size of the metallic powder covers both particle size (i.e. 0.1-30 μm) and the ultrafine inorganic powder. The metallic powder contained in the conductive paste, is more than 85 wt% (col 13 Table 1).

The conductive paste is bonded to the connecting member in the through holes by a degree of surface roughness (i.e. a porous surface), as such created an anchor effect (col 7 L 52-55).

The two printed wiring boards (305) are placed onto both sides of the connecting member. Both the connecting member as well as the printed wiring boards is made from a base material comprised of an inorganic or organic reinforcement and a thermosetting resin (col 10 L 45-67). Wherein the thermosetting resin is epoxy resin and the reinforcement can be a glass cloth (col 11 L 23-24).

Via holes are formed in the printed wiring boards and conductive patterns are formed onto the surfaces of the base materials (or interlaminer resin insulating layers). The conductive pattern is formed over the filled through hole (304) of the connecting member (309) (Fig. 3). Conductive layer is plated onto the surfaces and via holes of the printed wiring boards for electrically connecting with the connecting member.

Nakatani clearly teaches the present invention.

6. Claims 1-20, 23-26, 28-33, 36-42, 48, 52-55, 58, 66, 68, 72, 81-83, 87-88 and 92 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hatakeyama et al (US 5972482).

Hakateyama also teaches a multilayer printed circuit board comprised of a core layer (611) and two printed wiring board (609, 610) (Fig. 6).

The core layer is analogous to the claimed connecting member. The core layer is a resin impregnated fiber sheet substrate with through holes formed in the thickness direction. A conductive resin is filled into the through holes (col 1 L 63-col 2 L 4). The core layer is made from a porous substrate and that there exist some voids on the surface of the through holes, the conductive resin oozed into the surface voids (col 6 L 43-55 & Fig. 7a).

The conductive resin may also bonded to the surface of the through holes by the fibers sticking out from the resin matrix (col 6 L 64-67 & Fig. 7b). In both cases the examiner is taking the position that the through holes have a roughened surface.

The conductive resin is comprised of metallic particulates in an amount from 80 to 92.5 wt% and that the metallic particulates has an average diameter from 0.2 to 20 μm (col 5 L 40-45).

A metal foil is formed over the core layer surfaces and over the through hole filled with conductive resin (col 5 L 64-67). A plurality of printed wiring boards can be placed on both sides of the core layer to form a multilayer printed circuit board (col 6 L 28-42).

The printed wiring boards comprised of conductive surface patterns and conductive via holes are electrically connected to the conductive resin filled through holes. Furthermore, the conductive via holes are directly above the through hole (Figs. 5(f)-5(h)).

Hatakeyama clearly teaches the present invention.

7. Claims 1-2, 4-5, 7-8, 11, 12-13, 16, 17, 19, 20-21, 24, 25, 29, 30-32, 33, 37, 38-42, 46-67, 87-88 and 92 are rejected under 35 U.S.C. 102(b) as being anticipated by Yasue et al (US 6010768).

Yasue discloses a multilayer printed circuit board comprised of an insulating layers, conductor circuits, through holes and a resin filler.

Through holes (13) are formed in the insulating layer and conductor circuits are formed on both surfaces of the insulating layer (Fig. 7A). The surfaces of the through holes are first formed with a conductor metal, then the through holes are roughened by forming a needle-like alloy layer. A resin filler (14) is used to filled the roughened through holes (col 14 L 5-11 & Fig. 7(B)). The examiner is taking the position the insulating layer (1) being the substrate analogous to the claimed substrate and the insulating layers (2) are analogous to the claimed interlaminer insulating layer. The substrate (1) is a glass-epoxy resin layer (col 1 L 37-38).

Additional insulating layers (2) and conductor circuits are used to form over both surfaces of the substrate to form a multilayer structure (Figs. 3A-3I, col 3 L 13-18).

The resin filler (14) is filled in to the roughened through holes of the substrate (1). The resin filler (14) is comprised of bisphenol type epoxy resin and inorganic filler ( col

11 L 25-26, col 12 L 58-59, col 13 L 1-2 & L 10-12). The amount of inorganic filler is about 1-2 times of the bisphenol type epoxy resin (col 13 L 10-12). The inorganic fillers are ceramic particles such as silica, alumina, mullite, etc. (col 13 L 1-3). The average particle size ranges from 0.5-2 μm ( or 500-2000 nm) (col 13 L 4-6). The examiner is taking the position that Yasue's inorganic filler overlaps the claimed limitation of the ultra-fine inorganic powder sizes or 1-1000 nm. Since the resin filler does not include a metallic filler, the filler is non-conductive.

Conductor layers (5, 6) are formed onto the surfaces and through holes of the insulating layers (2) (Figs. 1A & 1B). The conductor layer (5) is covering the filled through hole of the substrate (1) (Figs. 3H & 3I).

***Claim Rejections - 35 USC § 103***

8. Claims 1-92 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasue et al (US 6010768) or Nakatani et al (US 5484647) or Hatakeyama et al (5972482).

All three prior art teach the concept of the present invention, but is silent about having a roughened layer formed on the surface and lateral sides of the conductor circuit over the through hole nor the substrate layer (or the connecting member) is a multilayer structure.

In view of the prior art teachings, one skill in the art would modify the prior art structure without departing form the main idea because such modification are just matter of design choice and that clearly applicant's invention is within the same concept of Yasue, Nakatani and Hatakeyama.

***Double Patenting***

9. Claims 1-92 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-55 of U.S. Patent No. 6,376,052. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are structurally similar and materially the same.

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cathy Lam whose telephone number is (571) 272-1538. The examiner can normally be reached on 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jennifer McNeil can be reached on (571) 272-1540. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cathy Lam

Cathy Lam
Primary Examiner
Art Unit 1775

cfl
August 17, 2006